

FEATURES

- ESD Protection Exceeds
 - ±15-kV Human-Body Model (HBM)
 - ±8-kV IEC 61000-4-2 Contact Discharge
 - ±15-kV IEC 61000-4-2 Air-Gap Discharge
- Low 1.5-pF Input Capacitance
- Low 1-nA (Max) Leakage Current
- Low 1-nA Supply Current
- 0.9-V to 5.5-V Supply-Voltage Range
- 3-Channel Device
- Space-Saving DRL, DRY, and QFN Package Options
- Alternate 2-, 4-, and 6-Channel Options
Available: TPD2E001, TPD4E001, and TPD6E001

APPLICATIONS

- USB 2.0
- Ethernet
- FireWire™
- Video
- Cell Phones
- SVGA Video Connections
- Glucosemeters

DESCRIPTION/ORDERING INFORMATION

The TPD3E001 is a low-capacitance ±15-kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND. The TPD3E001 protects against ESD pulses up to ±15-kV Human-Body Model (HBM), ±8-kV Contact Discharge, and ±15-kV Air-Gap Discharge, as specified in IEC 61000-4-2. This device has a 1.5-pF capacitance per channel, making it ideal for use in high-speed data IO interfaces.

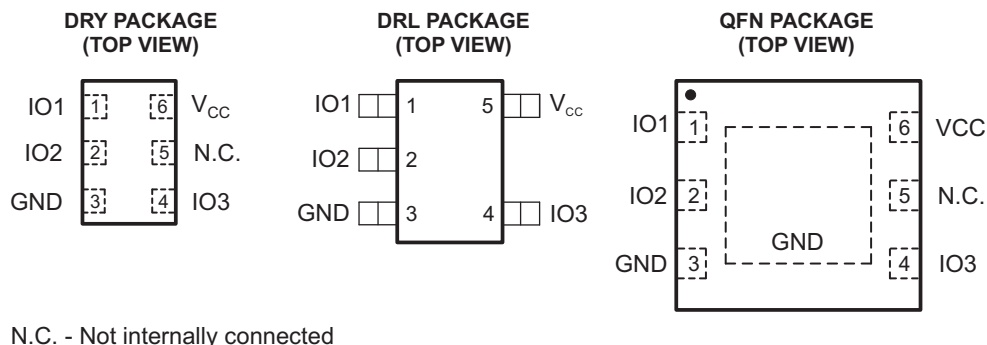
The TPD3E001 is a triple-ESD structure designed for USB On-the-Go (OTG) and video applications.

The TPD3E001 is available in DRL, DRY, and thin QFN packages and is specified for –40°C to 85°C operation.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	1.6 × 1.6 SOP – DRL	TPD3E001DRLR	2BR
	1.45 × 1 SON – DRY	TPD3E001DRYR	2B
	3 × 3 QFN – DRS	TPD3E001DRSR	ZWL

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



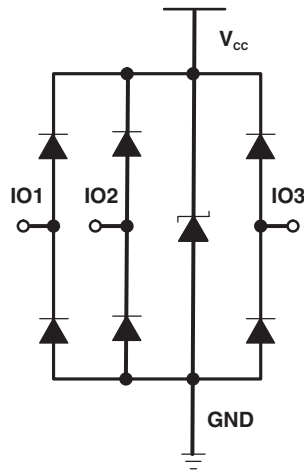
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FireWire is a trademark of Apple Computer, Inc.

TPD3E001
LOW-CAPACITANCE 3-CHANNEL ± 15 -kV ESD-PROTECTION ARRAY
FOR HIGH-SPEED DATA INTERFACES

SLLS683D–JULY 2006–REVISED APRIL 2007

LOGIC BLOCK DIAGRAM



PIN DESCRIPTION

DRL NO.	DRY NO.	DRS NO.	NAME	FUNCTION
1, 2, 4	1, 2, 4	1, 2, 4	IOx	ESD-protected channel
3	3	3	GND	Ground
5	6	6	V _{CC}	Power-supply input. Bypass V _{CC} to GND with a 0.1- μ F ceramic capacitor.
	5	5	N.C.	No connection. Not internally connected.
		EP	EP	Exposed pad. Connect to GND.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}		-0.3	7	V
V_{IO}		-0.3	$V_{CC} + 0.3$	V
T_{stg}	Storage temperature range	-65	150	°C
T_J	Junction temperature		150	°C
Bump temperature (soldering)	Infrared (15 s)		220	°C
	Vapor phase (60 s)		215	
Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

$V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	100	nA
V_F	Diode forward voltage	$I_F = 10\text{ mA}$		0.65		0.95	V
VBR	Breakdown Voltage	$I_{BR} = 10\text{ mA}$		11			V
V_C	Channel clamp voltage ⁽²⁾	$T_A = 25^\circ\text{C}$, $\pm 15\text{-kV HBM}$, $I_F = 10\text{ A}$	Positive transients			$V_{CC} + 25$	V
			Negative transients			-25	
		$T_A = 25^\circ\text{C}$, $\pm 8\text{-kV Contact Discharge}$ (IEC 61000-4-2), $I_F = 24\text{ A}$	Positive transients			$V_{CC} + 60$	
			Negative transients			-60	
		$T_A = 25^\circ\text{C}$, $\pm 15\text{-kV Air-Gap Discharge}$ (IEC 61000-4-2), $I_F = 45\text{ A}$	Positive transients			$V_{CC} + 100$	
			Negative transients			-100	
$I_{i/o}$	Channel leakage current	$V_{i/o} = \text{GND or } V_{CC}$				± 1	nA
$C_{i/o}$	Channel input capacitance	$V_{CC} = 5\text{ V}$, bias of $V_{CC}/2$			1.5		pF

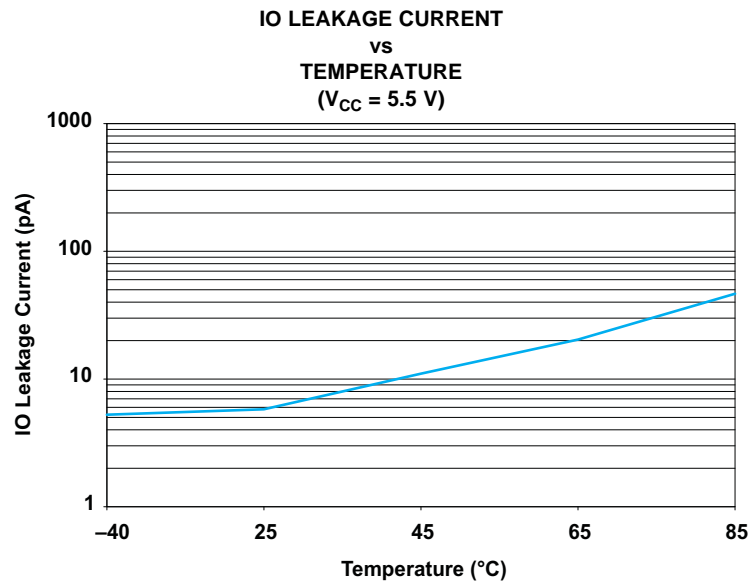
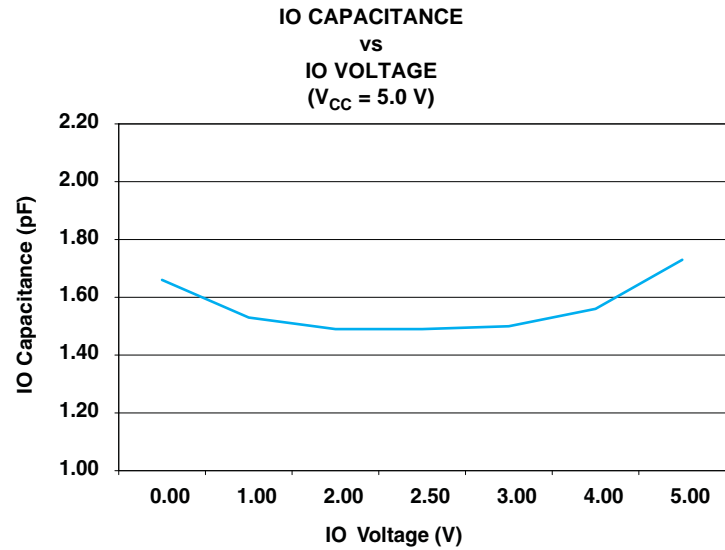
(1) Typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) Channel clamp voltage is not production tested.

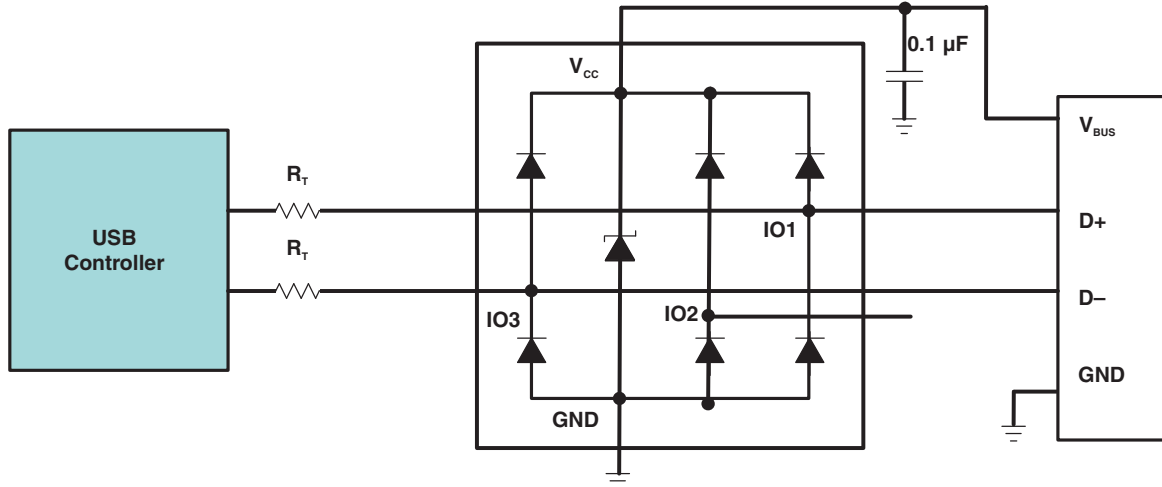
ESD Protection

PARAMETER	TYP	UNIT
HBM	± 15	kV
IEC 61000-4-2 Contact Discharge	± 8	kV
IEC 61000-4-2 Air-Gap Discharge	± 15	kV

TYPICAL OPERATING CHARACTERISTICS



APPLICATION INFORMATION



Detailed Description

When placed near the connector, the TPD3E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD3E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD3E001 solution close to the connector. This allows the TPD3E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1- μF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD3E001 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating.
5. The V_{CC} pin can be connected in two different ways:
 - a. If the V_{CC} pin is connected to the system power supply, the TPD3E001 works as a transient suppressor for any signal swing above $V_{CC} + V_F$. A 0.1- μF capacitor on the device V_{CC} pin is recommended for ESD bypass.
 - b. If the V_{CC} pin is not connected to the system power supply, the TPD3E001 can tolerate higher signal swing in the range up to 10 V. Please note that a 0.1- μF capacitor is still recommended at the V_{CC} pin for ESD bypass.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPD3E001DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD3E001DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD3E001DRSR	ACTIVE	SON	DRS	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPD3E001DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPD3E001DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

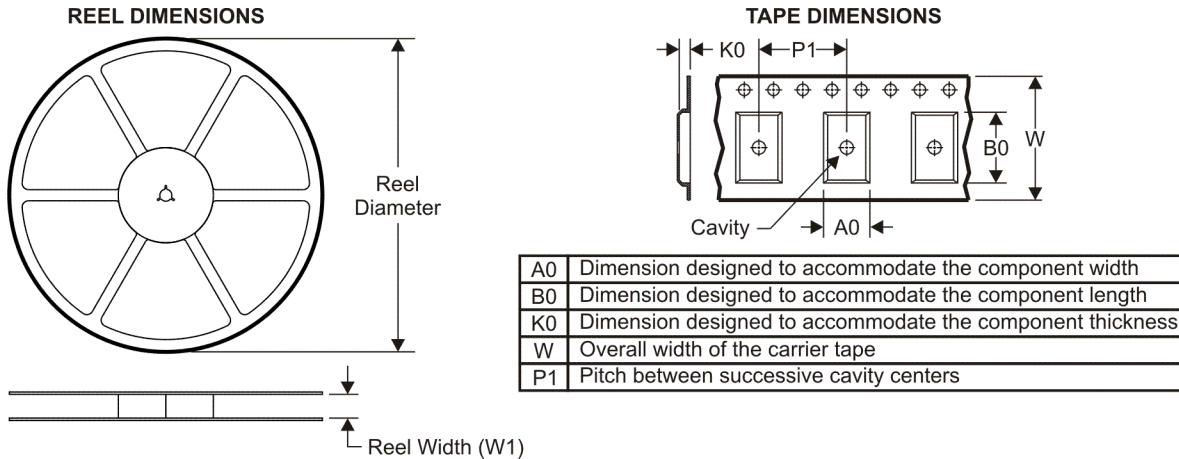
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

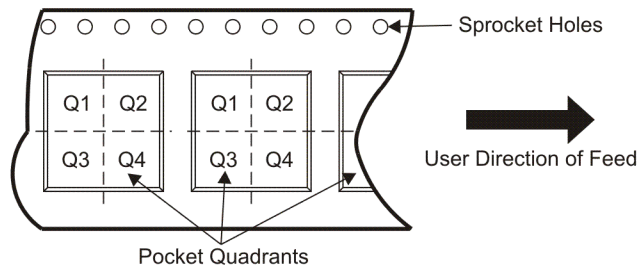
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



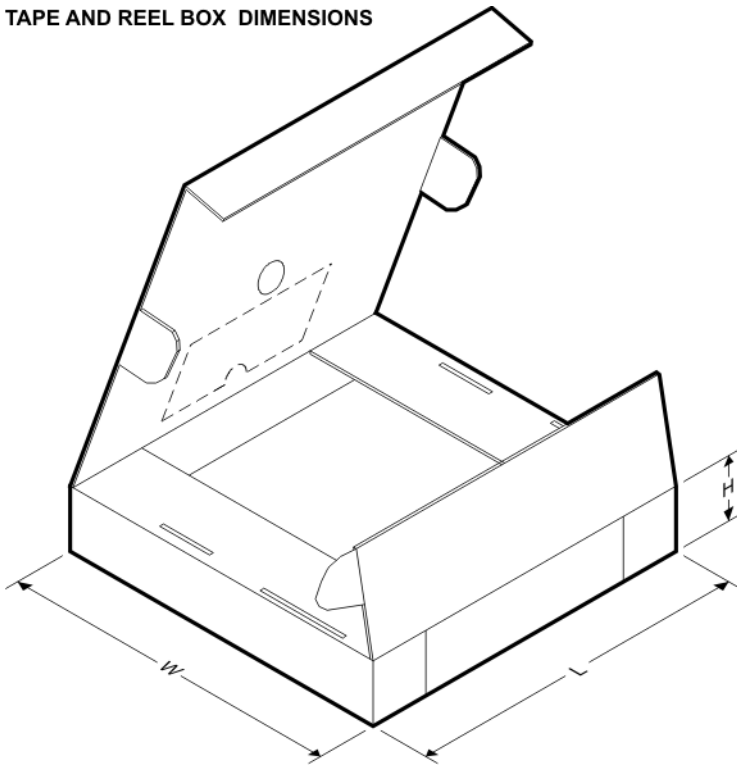
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

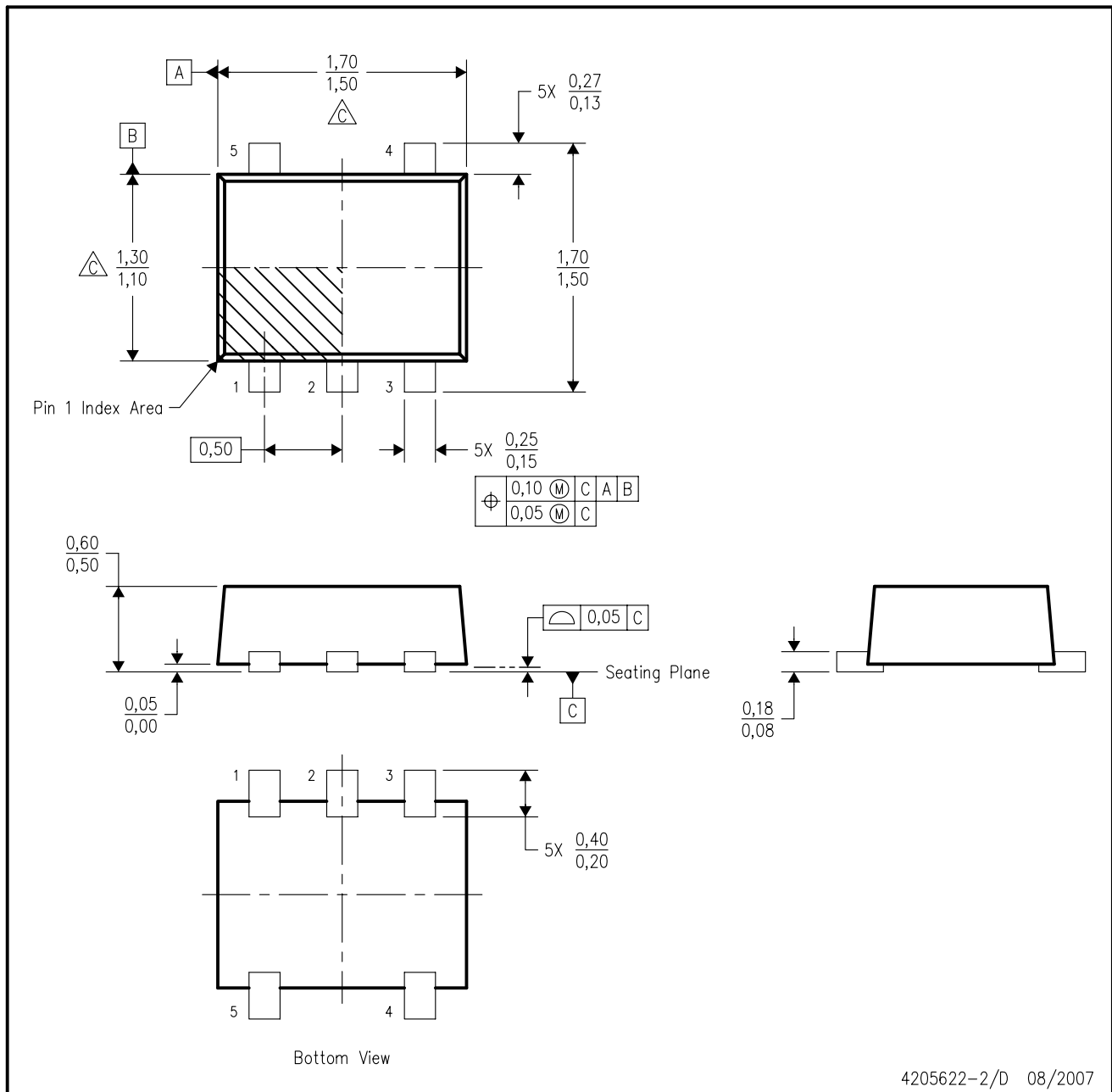
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3E001DRLR	SOT	DRL	5	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3
TPD3E001DRSR	SON	DRS	6	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPD3E001DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3E001DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
TPD3E001DRSR	SON	DRS	6	1000	346.0	346.0	29.0
TPD3E001DRYR	SON	DRY	6	5000	220.0	205.0	50.0

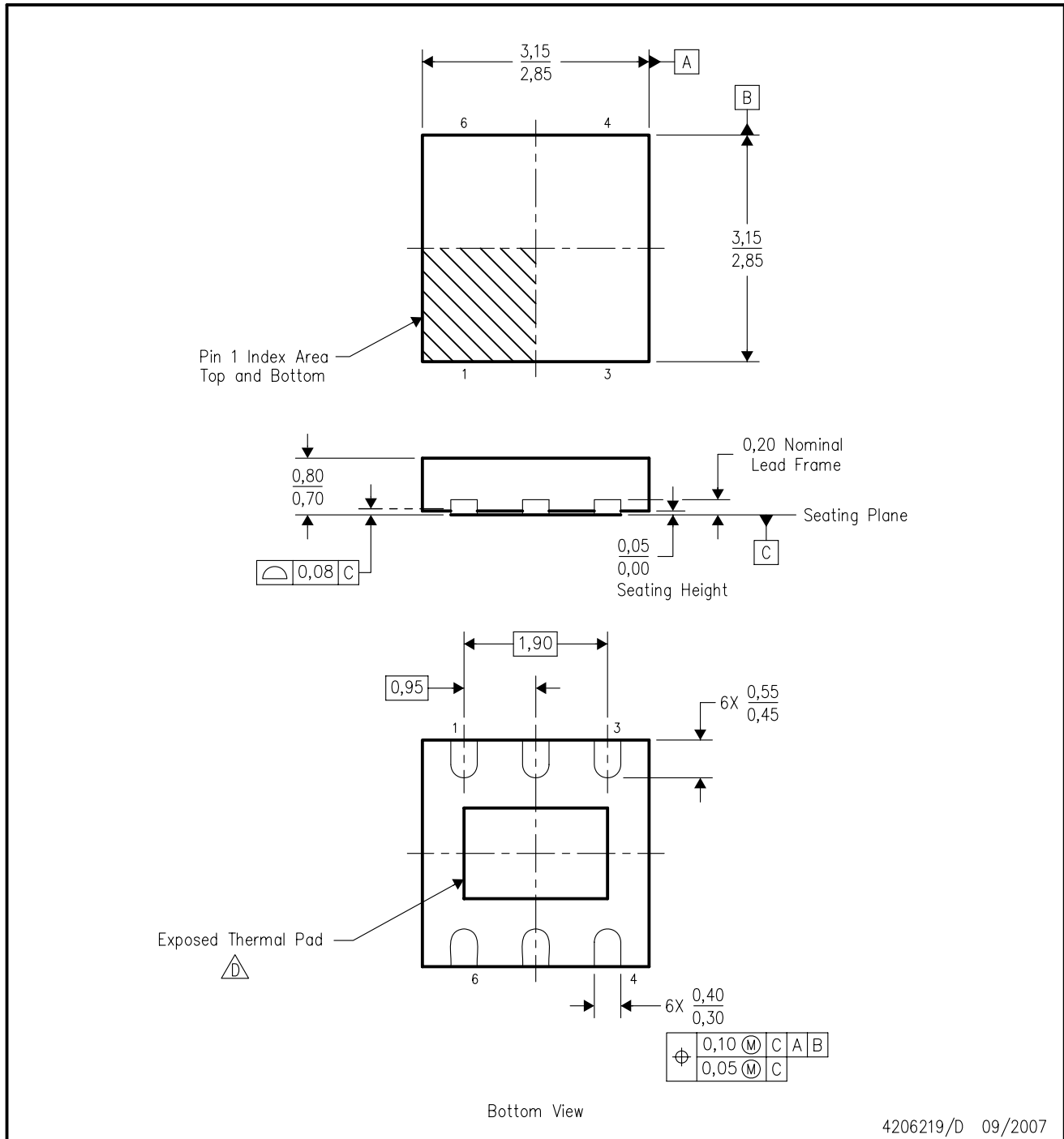



4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

DRS (S-PDSO-N6)

PLASTIC SMALL OUTLINE



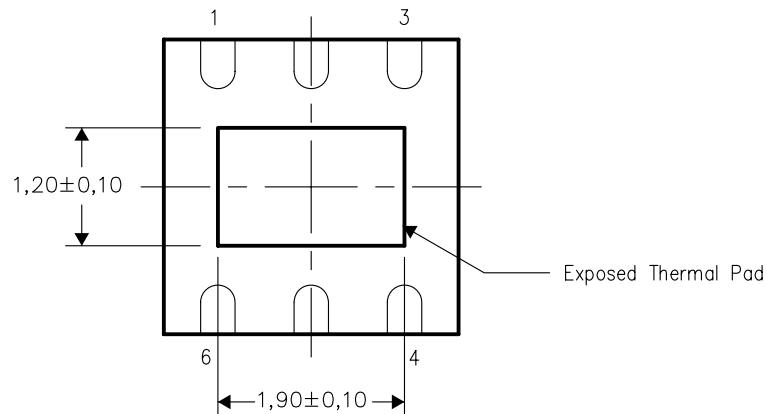
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

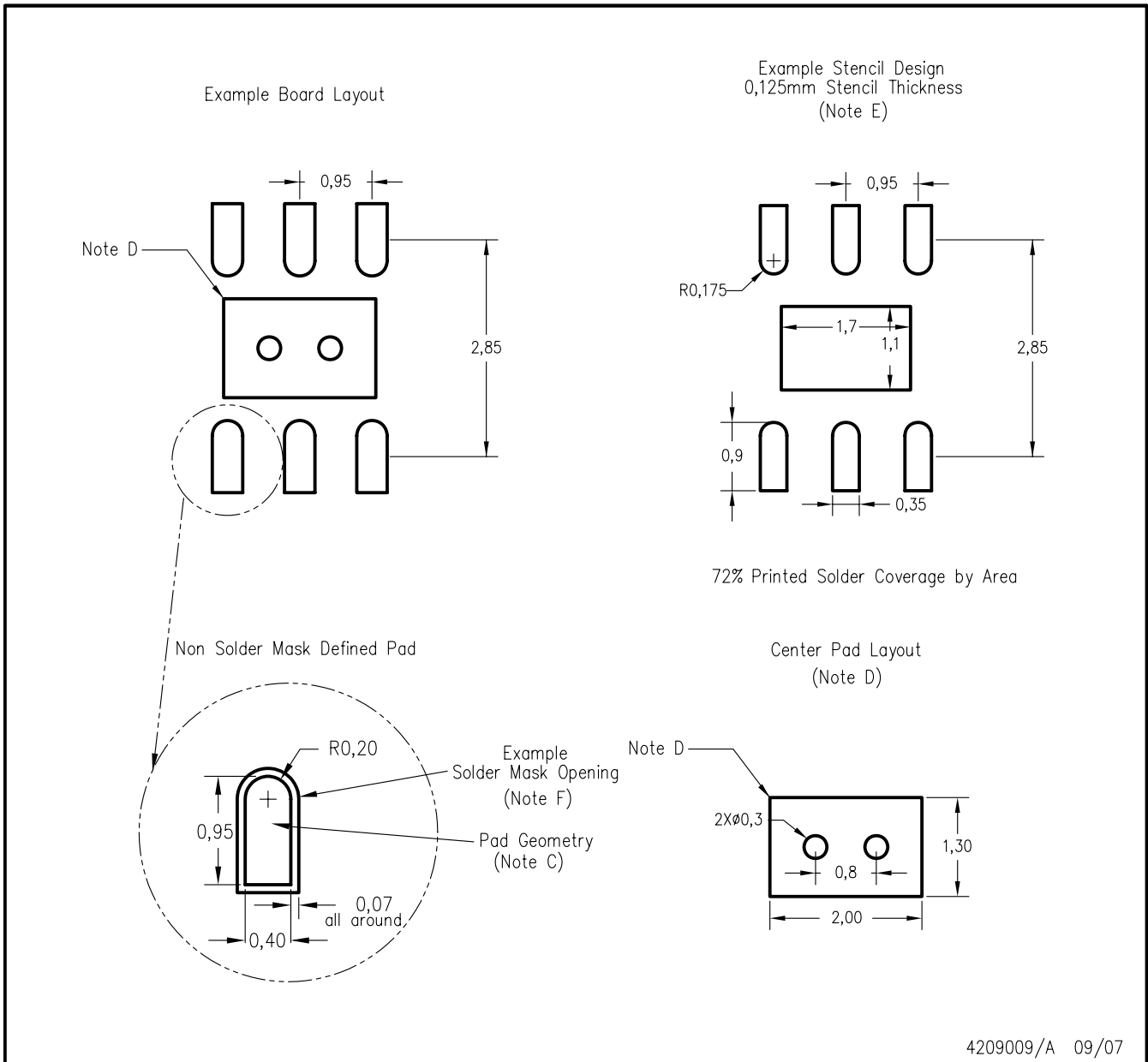


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

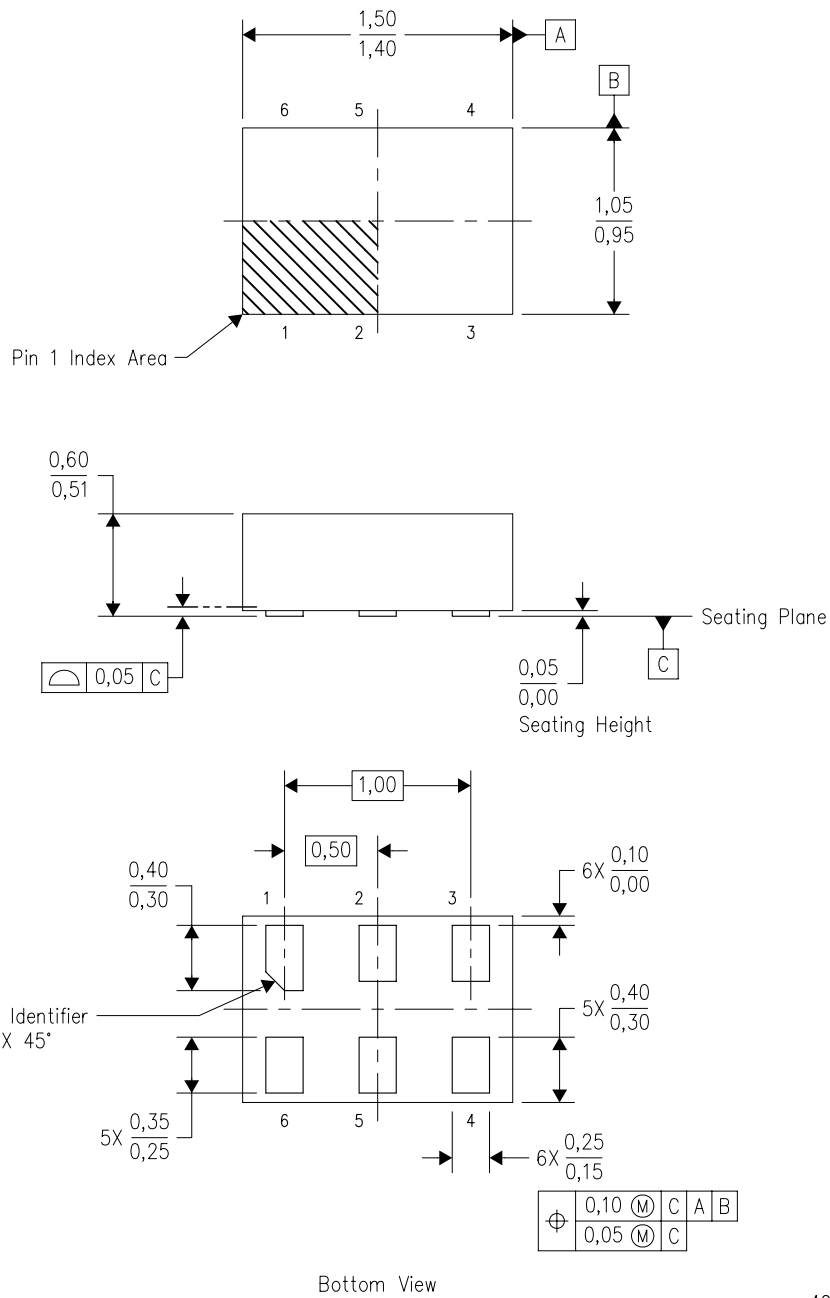
DRS (S-PDSO-N6)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

DRY (R-PDSO-N6)

PLASTIC SMALL OUTLINE



4207181/B 12/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. This package complies to JEDEC MO-287 variation UFAD.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated